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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)
	10/068,276	KUNG ET AL.
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 29-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 29-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 and 29-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Schueller (US Pat. 5866949).

Regarding claim 1, Brooks et al. disclose a tape ball grid array (TBGA) package comprising:

- a dielectric layer/tape (16/18 in Fig. 2) having a first/top side and a second/bottom side and a plurality of via holes (34 in Fig. 2) that pass through the dielectric layer
- a patterned first metallic layer (22 in Fig. 2) over the first side of the dielectric layer such that on end of the via holes is closed to form a plurality of blind holes (34 in Fig. 2)

- a patterned second metallic layer (20/24 in Fig. 2) over the second side of the dielectric layer, the second metallic layer including conductive contact element site/pad (24 in Fig. 2) connecting the respective via holes and serving as a ground, power or reference/signal transmission plane/layer depending on application requirements (Col. 7, line 1-5)
- a patterned first solder mask layer (8 in Fig. 2) over the first metallic layer exposing a portion of the metallic layer to serve as a plurality of contact points and conductive traces/paths (46 and 32 in Fig. 1 and 2; Col. 5, line 65- Col. 6, line 35)
- a patterned second solder mask layer (6 in Fig. 2) over the second metallic layer exposing a portion of the metallic layer and conductive element sites (Col. 6, line 2)
- a plurality of conductive elements/solder balls (26 in Fig. 2) being placed on the conductive element sites at the blind holes with one end protruding out from the surface of the second solder mask (Col. 5, line 40; Col. 6, line 10-16)
- the solder balls, the first metallic layer and the second metallic layers being electrically connected (Fig. 2; Col. 5, line 25-65), and
- a chip having an active/top surface including a plurality of bonding pads (14a in Fig. 2) and a back surface, the chip being electrically connected to various inner pads/contact points (46 in Fig. 2) on the first/top side of the tape

(Fig. 1 and 2; Col. 5, line 15- Col. 7, line 25).

Brooks et al. fail to teach the blind via holes having an open end such that the solder balls are inserted into the blind via holes.

Schueller teaches a flexible BGA package having via holes/blind vias and solder balls where the via hole (55 in Fig. 3B) has an open end (see the end at pad 59b in Fig. 3B) such that the solder balls (54a in Fig. 3B) are inserted into the blind via holes at the open end to provide the desired ground connection (Col. 9, line 25-33).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the blind via holes having an open end such that the solder balls are inserted into the blind via holes as taught by Schueller so that the desired ground, power or signal routing can be achieved and the thermal dissipation can be improved in Brooks et al's package.

Regarding claim 2, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. further teach the dielectric layer (16/18 in Fig. 2) including polyimide material (Col. 5, line 26).

Regarding claim 3, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. further teach the second metallic layer (20/24 in Fig. 2) serving as ground or power plane/layer (Col. 7, line 1-10).

Regarding claim 4, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. further teach the first metallic layer (20 in Fig. 2) serving as ground, power or reference/signal transmission plane/layer depending on application requirements (Col. 6, line 65-Col. 7, line 1-10).

Regarding claim 5, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. further teach the material of the first and second metallic layers (22 and 24/20 respectively in Fig. 2) constituting copper material (Col. 5, line 28).

Regarding claim 6, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. further teach the first and second metallic layers (22 and 24/20 respectively in Fig. 2) further including metallic alloy layers (Col. 5, line 53).

Regarding claim 7, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. further teach the first and second metallic layers (22 and 24/20 respectively in Fig. 2) constituting the nickel-gold alloy material (Col. 5, line 53).

Regarding claim 8, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. teach the chip having the plurality of bonding pads on the active surface (14a in Fig. 2; Col. 7, line 11).

Regarding claim 9, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, and Brooks et al. further teach the package including:

- a plurality of conductive wires and packaging material (48 and 54 respectively in Fig. 2)
- the back side of the chip being attached using a dielectric adhesive (Col. 6, line 58)
- the conductive wires connecting the bonding pads and corresponding contact points on the tape (48/14a/46 in Fig. 1 and 2), and
- the packaging material (54 in Fig. 2) enclosing the chip, conductive wires and contact points

(Col. 6, line 53- Col. 7, line 25).

Brooks et al. fail to teach the chip being attached to the first solder mask layer.

Schueller teaches using a dielectric adhesive such as polyimide/solder mask (64 in Fig. 3B) as a chip attachment material to reduce the stress and to improve reliability of solder joints (Col. 8, line 57; Col. 9, line 65- Col. 10, line 11).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the chip being attached to the first solder mask layer as taught by Schueller so that the chip adhesion and the reliability of the bonding /interconnection can be improved in Brooks et al's package.

Regarding claim 10, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. further teach using a composite adhesive/heat sink/stiffener frame (40/50 in Fig. 2) on the first solder mask surrounding the packaging material and the chip (Col. 6, line 17-52).

Regarding claim 29, Brooks et al. disclose a tape ball grid array (TBGA) package comprising:

- a dielectric layer/tape (16/18 in Fig. 2) having a first/top side and a second/bottom side and a plurality of via holes (34 in Fig. 2) that pass through the dielectric layer
- a patterned first metallic layer (22 in Fig. 2) over the first side of the dielectric layer such that on end of the via holes is closed to form a plurality of blind holes (34 in Fig. 2)
- a patterned second metallic layer (20/24 in Fig. 2) over the second side of the dielectric layer, the second metallic layer including conductive contact element site/pad (24 in Fig. 2) connecting the respective via holes
- the first or second metallic layers and respective contact element sites/pads being selected to serve as a ground, power or reference/signal transmission plane/layer depending on application requirements through respective vias (Col. 6, line 65- Col. 7, line 10)
- a patterned first solder mask layer (8 in Fig. 2) over the first metallic layer exposing a portion of the metallic layer to serve as a plurality of contact points and conductive traces/paths (46 and 32 in Fig. 1 and 2; Col. 5, line 65- Col. 6, line 35)
- a patterned second solder mask layer (6 in Fig. 2) over the second metallic layer exposing a portion of the metallic layer and conductive element sites (Col. 6, line 2)

- a plurality of conductive elements/solder balls (26 in Fig. 2) being placed on the conductive element sites at the blind holes with one end protruding out from the surface of the second solder mask (Col. 5, line 40; Col. 6, line 10-16)
- the solder balls/plurality of second solder balls electrically connecting the first metallic layer and the second metallic layer (Fig. 2; Col. 5, line 25-65), and
- a chip having an active/top surface including a plurality of bonding pads (14a in Fig. 2) and a back surface, the chip being electrically connected to various inner pads/contact points (46 in Fig. 2) on the first/top side of the tape

(Fig. 1 and 2; Col. 5, line 15- Col. 7, line 25).

Brooks et al. fail to teach:

a) the solder balls including a plurality of first and second solder balls, the solder balls being inserted into a portion of the blind via holes, and

b) a plurality of first solder balls electrically connecting the first metallic layer and the plurality of second solder balls electrically connecting the first and second metallic layers.

a) Schueller teaches a flexible BGA package comprising a variety of solder ball mounting configurations including an embodiment in Fig. 3B where the solder balls (54a in Fig. 3B) are inserted into a portion of the via holes (55 in Fig. 3B; Col. 9, line 26).

b) Schueller further teaches the BGA interconnect structure comprising a plurality of metal layers having respective solder ball/bonding pad connections to provide an improved shielding, reduced cross-talk and the desired ground/power connection (Col.

9, line 20-25). The BGA configuration further comprises a plurality of solder balls (54a in Fig. 3B) electrically connecting the first and second metallic layers (53 and 59b respectively in Fig. 3B; Col. 9, lines 25-28) and a plurality of remaining solder balls electrically connecting another metallic layer (see solder balls 54 and metallization 59 respectively in Fig. 3B) to achieve the desire power/ground routing.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the plurality of first and second solder balls being inserted into a portion of the blind via holes, the plurality of first solder balls electrically connecting the first metallic layer and the plurality of second solder balls electrically connecting the first and second metallic layers as taught by Schueller so that the desired ground, power or signal routing can be achieved and the thermal dissipation and shielding can be improved in Brooks et al's package.

Regarding claim 30, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 29 above, wherein Brooks et al. further teach the dielectric layer (16/18 in Fig. 2) being a polyimide material (Col. 5, line 26).

Regarding claim 31, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 29 above, wherein Brooks et al. further teach the material of the first and second metallic layers (22 and 24/20 respectively in Fig. 2) being copper (Col. 5, line 28).

Regarding claims 32 and 33, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 29 above, wherein Brooks et al. further teach the first and second metallic layers (22 and 24/20 respectively in Fig. 2) being metallic alloy layers (Col. 5, line 53) constituting the nickel-gold alloy material (Col. 5, line 53).

Regarding claim 34, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claim 29 above, wherein Brooks et al. teach the chip having the plurality of bonding pads on the active surface (14a in Fig. 2; Col. 7, line 11).

Regarding claim 35, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claims 29 and 34 above, and Brooks et al. further teach the package including:

- a plurality of conductive wires and packaging material (48 and 54 respectively in Fig. 2)
- the back side of the chip being attached using a dielectric adhesive (Col. 6, line 58)
- the conductive wires connecting the bonding pads and corresponding contact points on the tape (48/14a/46 in Fig. 1 and 2), and
- the packaging material (54 in Fig. 2) enclosing the chip, conductive wires and contact points

(Col. 6, line 53- Col. 7, line 25).

Brooks et al. and Schueller fail to teach the chip being attached to the first solder mask layer.

Schueller further teaches using a dielectric adhesive such as polyimide/solder mask (64 in Fig. 3B) as a chip attachment material to reduce the stress and to improve reliability of solder joints (Col. 8, line 57; Col. 9, line 65- Col. 10, line 11).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the chip being attached to the first solder mask layer as taught by Schueller so that the chip adhesion and the reliability of the bonding /interconnection can be improved in Brooks et al's package.

Regarding claim 36, Brooks et al. and Schueller teach substantially the entire claimed structure as applied to claims 29, 34 and 35 above, wherein Brooks et al. further teach a composite adhesive/heat sink/stiffener frame (40/50 in Fig. 2) being on the first solder mask surrounding the packaging material and the chip (Col. 6, line 17-52).

3. Claims 11-13 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) and Schueller (US Pat. 5866949) as applied to claims 1, 8, 29 and 34 above, and further in view of Dordi (US Pat. 5835355).

Regarding claim 11, Brooks et al. and Schueller teach substantially the entire claimed structure, as applied to claims 1 and 8 above, except a plurality of bumps protruding from the bonding pads and the bumps correspond in position to various contact points.

Dordi teaches using a TBGA package where an active surface/bottom of a chip (12 in Fig. 1) has a plurality of interconnection points comprising pads (not numerically referenced in Fig. 1; Col. 4, line 46) and bonding bumps (14 in Fig. 1) protruding from

the respective interconnection points corresponding in position to various/selected traces/contact points (Col. 4, lines 45-60).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the plurality of bumps protruding from the bonding pads and the bumps corresponding in position to various contact points chip as taught by Dordi so that the package height can be reduced and the reliability of the bonding /interconnection can be improved in Brooks et al. and Schueller's package.

Regarding claim 12, Brooks et al. and Schueller teach substantially the entire claimed structure, as applied to claims 1, 8 and 11 above, except an underfilling material enclosing the bonding pads, the bumps and the contact points.

Dordi teaches using the TBGA package having an encapsulant/underfill (13 in Fig. 1) sealing the bonding pads, the bumps and the respective contact points (Col. 5, line 15).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an underfilling material enclosing the bonding pads, the bumps and the contact points as taught by Dordi so that the surface protection at the interconnection points can be improved and the reliability of the bonding /interconnection can be improved in Brooks et al. and Schueller's package.

Regarding claim 13, Brooks et al. and Schueller teach substantially the entire claimed structure, as applied to claims 1, 8, 10 and 11 above, including the stiffener (40/50 in Fig. 2) being on the first solder mask surrounding the chip (Col. 6, line 17-52).

Regarding claim 37, Brooks et al. and Schueller teach substantially the entire claimed structure, as applied to claims 29 and 34 above, except a plurality of bumps protruding from the bonding pads and the bumps correspond in position to various contact points.

Dordi teaches using a TBGA package where an active surface/bottom of a chip (12 in Fig. 1) has a plurality of interconnection points comprising pads (not numerically referenced in Fig. 1; Col. 4, line 46) and bonding bumps (14 in Fig. 1) protruding from the respective interconnection points corresponding in position to various/selected traces/contact points (Col. 4, lines 45-60).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the plurality of bumps protruding from the bonding pads and the bumps corresponding in position to various contact points chip as taught by Dordi so that the package height can be reduced and the reliability of the bonding /interconnection can be improved in Brooks et al. and Schueller's package.

Regarding claim 38, Brooks et al. and Schueller teach substantially the entire claimed structure, as applied to claims 29, 34 and 37 above, except an underfilling material enclosing the bonding pads, the bumps and the contact points.

Dordi teaches using the TBGA package having an encapsulant/underfill (13 in Fig. 1) sealing the bonding pads, the bumps and the respective contact points (Col. 5, line 15).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an underfilling material enclosing the bonding pads, the bumps and the contact points as taught by Dordi so that the surface protection at

the interconnection points can be improved and the reliability of the bonding /interconnection can be improved in Brooks et al. and Schueller's package.

Regarding claim 39, Brooks et al. and Schueller teach substantially the entire claimed structure, as applied to claims 29, 34, 37 and 38 above, wherein Brooks et al. further teach the stiffener (40/50 in Fig. 2) being on the first solder mask surrounding the chip (Col. 6, line 17-52).

Response to Arguments

4. Applicant's arguments filed on 07-08-03 have been fully considered but they are not persuasive.

A. Applicant contends that pad type conductive connection of the solder balls in Brooks et al. is different than that claimed and the combination with Schueller is not proper since Schueller has the dielectric layer only on one side of the metallic layer.

However, Schueller's solder ball structure inserting the solder balls into the blind vias (see Fig. 3B) to provide the connection to respective metallization and to achieve the desired ground connection and thermal dissipation is applied to the solder ball/pad structure in Brooks et al's BGA package having the dielectric tape with metallic layers on both sides.

B. Applicant contends that Schueller's solder balls do not pass through the second metal layer and stop at the patterned first metal layer.

However, Schueller teaches the solder balls (54a in Fig. 3B) passing through the metallization 59b and stopping at the patterned metallization 50 in Fig. 3B.

C. Applicant contends that Schueller's solder balls are used for ground connection only while the invention claims signal and ground/power solder balls.

However, Brooks et al. teach the first and second metallic layers and respective contact element sites/pads being selected to provide the ground, power or reference/signal connections depending on application requirements through respective vias and solder balls (Col. 6, line 65- Col. 7, line 10; Col. 5, lines 25-65). Therefore, Brooks et al. is combined with Schueller to incorporate Schueller's blind via configuration having inserted solder balls.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
09-16-03

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800